ReChip: Embedded FPGA SoC as Reusable and Repairable Chips for Sustainable Computing

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Carbon footprint is the indicator of climate change, and the effect is skyrocketing with the advent of computation-hungry AI and machine-learning applications. The semiconductor industry is on the run to decrease its operating carbon footprint through decades of efforts in sustainable accelerators like ASICs and FPGAs. While ASICs provide high performance, they demand redesign from scratch for each new application, producing more carbon footprints throughout the planning, design and manufacturing process. FPGAs offer reusability with a smaller footprint, although they have lower performance. Moreover, with the increasing demand for AI hardware, the design, production, and packaging add more embodied emissions. As a result, there is a need for more initiatives towards sustainable and green computing than ever before, which can provide reusability, repairability, reprogrammablity, and recyclability without compromising high performance. Previous studies have leveraged the reconfigurability of FPGA as a solution for reusability and compared the embodied carbon footprint between ASIC and FPGA. However, these methods suffer from significantly higher area overhead and performance bottleneck. This study presents ReChip—a reusable and repairable System-on-chip (SoC) designed by combining embedded Field Programmable Gate Array (eFPGA) and application-specific integrated circuit (ASIC). By reducing carbon emissions via two primary strategies—"reducing" new manufacturing by "reusing" pre-designed eFPGA IP blocks and implementing hierarchical approaches to system design—ReChip offers substantial potential to promote green computing. The unique characteristic of the proposed hybrid SoC is that it not only utilizes the reconfigurability of FPGA but also leverages the high performance that ASIC can offer, making ReChip a lucrative sustainable alternative for performance intensive application. Compared to ASICs and FPGAs, the paper assesses scenarios in which the sustainable advantages of this versatile chip exceed operational and embodied carbon costs, establishing ReChip as a greener alternative for hardware acceleration. According to experimental findings, the proposed hybrid SoC outperforms previously manufactured heterogeneous reconfigurable SoCs as an energy-efficient solution for various applications.

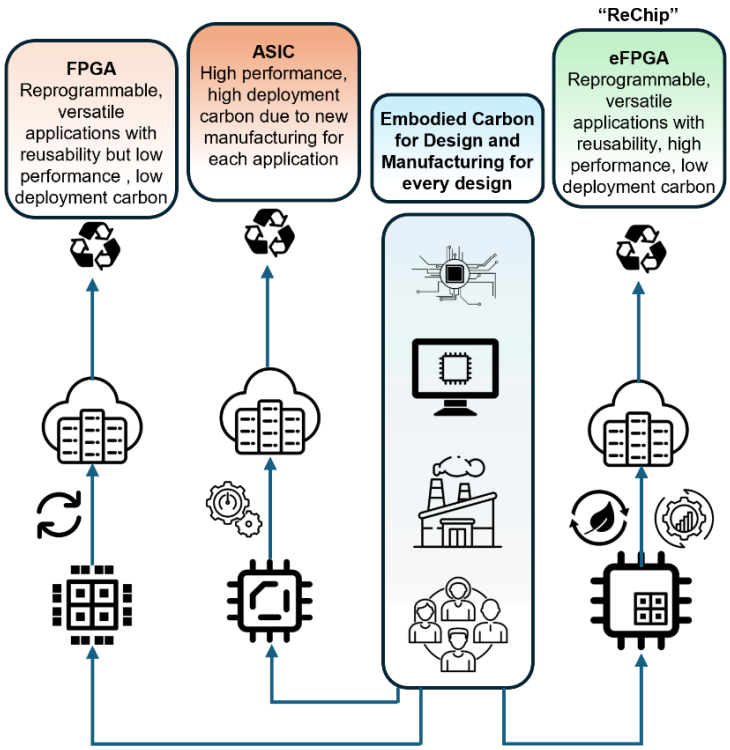

Fig 1: Comparison of Reusable and Repairable eFPGA ('ReChip') with ASIC and FPGA for sustainable computing ecosystem.

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